It is important to realize that a DAC is just one “link” among other links in a circuit design. Any circuit board’s “chain” is only as strong as each link, so this article will focus on design practices to make your DAC circuit as strong as possible. First, this article will discuss the system architecture and the selection of a DAC based on its key characteristics. Then, the article will cover the selection of a DAC reference and some design guidelines including the use of references and output conditioning. The last section of the article will review techniques for preventing noise and best practices for PCB layout.

ARCHITECTURE AND SELECTING A DAC
Before building the walls for a house, a foundation must be laid. For electrical designers, the foundation is the circuit architecture. In military, aviation, and other applications, a high level system specification drives the creation of the architecture. Even though simple applications do not have a system specification, every designer can benefit by understanding how the DAC operates in the architecture. An easy way to do this is to draw a block diagram of the architecture. Let’s take a look at Figure 1, a simple diagram which represents one way to architect a handheld audio player.

![Figure 1 - Architecture Diagram](image)

As shown, the microcontroller will control and send data to the DAC. Based on the input data code, the DAC will output an analog voltage to an audio amplifier to adjust the volume/gain. Then the audio amplifier will drive the loudspeaker with a gain set by the DAC. From this simple diagram, you can see that the DAC will require:

- I2C interface
- Fast enough to support audio frequency range of 20Hz-20K Hz
- Supply voltage rails of 5V
- Power efficiency required due to battery source
With key requirements identified, the designer can start selecting an appropriate DAC. In selecting a DAC, a designer should review several manufacturers’ datasheets and use a highlighter to mark all key characteristics that meet the requirements as identified above. The DAC characteristics are contained in the datasheet’s Electrical Characteristics table and organized into sections such as Static Performance, Output Characteristics, Power Requirements, and Dynamic Characteristics. This link shows typical DAC datasheet ([http://www.national.com/ds/DA/DA C121S101.pdf](http://www.national.com/ds/DA/DA C121S101.pdf)) Below I will cover some of the most important parameters used in most typical applications.

### Interface

In many applications, the input data code is generated from a microcontroller, FPGA/CPLD, or other processor. More importantly, the design team will usually select the processor or microcontroller first - before any other component on a board. The reason can be existing software code, developmental tools, or even the experience of the software/hardware team. So while the basic DAC parameters discussed in the first article are important, the interface is often the most critical requirement. There are three common DAC interfaces to consider, as shown on Figure 2.

<table>
<thead>
<tr>
<th>Interface</th>
<th># Wires</th>
<th>Typical Data Rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parallel</td>
<td>8-16 data + 2-4 control/clock</td>
<td>Can support high data rates of 100+ Mbps - depends on device</td>
</tr>
<tr>
<td>I²C</td>
<td>2 wires - Data (SDA), Clock (SCL)</td>
<td>Various rates, but typically can reach 1Mbps</td>
</tr>
<tr>
<td>SPI</td>
<td>4 wires - Clock (SCLK), Data out (SDO), Data in (SDI), Chip Select (nCS)</td>
<td>Can reach 400Mbps</td>
</tr>
<tr>
<td>Microwire</td>
<td>3 wires - Clock (SCLK), Data In (DIN), Frame Sync (nSync)</td>
<td>Can reach 400Mbps</td>
</tr>
</tbody>
</table>

**Figure 2 - Interfaces comparison**

The **Parallel** interface uses separate wires for each signal bit and includes additional wires for control and clock signals. It is easy to implement on an IC, but requires a larger number of traces and pins. The speed of parallel interface depends on each particular DAC but support very high data rates. The **Inter-Integrated Chip (I²C)** serial bus was invented by Philips (NXP) and is the most popular serial bus used in microcontrollers. I²C supports uses a data rate of 100 kbps for standard mode but can support up to 1 Mbps on most microcontrollers. The **Serial Peripheral Interface Bus (SPI)** is a synchronous serial standard developed by Motorola and also available on many microcontrollers. It can support up to 400Mbps, with typical data rates of 1Mbps. One disadvantage of the SPI standard is that it is not as closely regulated as I²C which can result in devices with SPI interfaces that are not fully compatible. **Microwire** is a serial interface developed by National Semiconductor in the early 1980’s and is considered a predecessor and subset of SPI.

### Resolution

A DAC resolution, just like an ADC, is specified in the number of bits. The resolution, along with the DAC reference, determines the granularity of the output signal. In application such as calibration may require 16-bit resolution or more, while a circuit for voltage offset adjustment may only need a 10-bit DAC. As was demonstrated in the first article, the representation of the output signal will depend much on the resolution. DACs are available in
resolutions of 8 to 24 bits, and the designer should estimate how much granularity he really requires since higher resolution DACs of 16 bits cost significantly more.

**Settling Time**

Settling time is the time from a change in the input code until the DAC output signal is generated and remains within the specified tolerance of the final value. The characterization of settling time will vary across manufacturers, so it is important to review the test conditions used for each datasheet. For an application with DC or slow frequency signals (such as audio), the settling time is usually not a key requirement. However, if the DAC will provide a fast moving waveform for a T&M system, then the settling time may be the most critical requirement. Any designer should plan for a good margin between the max settling time and the time the signal is required at the output. Remember – specifications are given under certain testing conditions and your application conditions could be different! Good design margin applies to virtually every aspect of DAC design.

**Integral Non-Linearity (INL) and Differential Non-Linearity (DNL)**

A linear DAC should act as a perfect “mirror” reflecting exactly what is on the input. The non-linearity of a DAC is divided into two aspects - INL and DNL. INL is a measure of the deviation of each input code from a straight line through the input/output transfer function. DNL is a measure of the maximum deviation from the ideal step size of 1 LSB. An illustration of the impact on a DAC’s output is shown below in Figure 3.

![Figure 3 - Linearity](image)

If one can imagine a sinusoid waveform applied to the transfer function oriented from the horizontal axis, the output waveform should be a perfect replica. But with INL/DNL present, the sinusoid signal will appear distorted. This means the DAC output signal will not precisely represent the input code. In applications such as calibration systems or T&M, which require high precision, these characteristics are very important. But in other applications, such as adjusting simple DC step voltages for a LCD backlight, the linearity may not be a critical issue.

**Packaging and Power**

Packaging is an important issue and can limit the range of selection. For example, if the assembly line cannot support small Ball Grid Arrays (BGAs), those DACs without alternative packages must be eliminated from selection. Packaging also plays a role in the circuit’s thermal
profile. Each manufacturer should specify typical Theta Junction-to-Ambient ($\Theta_{JA}$) for the package. Along with maximum junction temperature and expected dissipated power, this value is used to plan the board’s thermal profile. The power consumption of a DAC is important in modern designs, but especially in battery or portable applications. A low power DAC can improve the overall thermal profile of a board and alleviate the need for heatsinks. For low power applications, the designer should look for DACs with typical power consumption of less than 2-3 mW per channel. Most new DACs have standby modes which can keep power consumption below 1uW. This can be an important differentiator in selection.

**DESIGN GUIDELINES**

The first step after DAC selection should be a thorough review of the datasheet. Datasheets should include a complete functional description, pin description, and applications section, plus reference diagrams that can be used as a starting point for your circuit. Also, existing reference designs and evaluation boards may be available on the DAC’s webpage. With those, it is easy to optimize the components for your application since eval boards are typically well-tested prior to public release.

**References and Power Supplies**

DACs which use the same pin for reference and power supply require a very quiet power supply source. Ideally the reference/power supply will have an accuracy of below 1%, but in many cases the DAC will need a more accurate reference. In this case, it may be challenging to find a power supply which has sufficient current output as well as high accuracy. Fortunately, many new DACs can operate with less than 50mA, which alleviates that constraint. An example of a voltage reference used with a low power DAC is shown on Figure 4. In DACs with separate power and reference lines, the same requirements in the datasheet should be followed. The separation of functions does allow more flexibility in power supplies, but has more complexity in the implementation.

![Figure 4 - Voltage Reference and DAC](image)

**DAC Output Conditioning**

While the DAC outputs can be connected directly to a load, in most cases the signal will require additional buffering or conditioning. This can be done with a non-inverting opamp set up as a voltage follower (buffer) or one with gain if needed. Figure 5 shows two ways to condition the output signal and add gain. The opamp is flexible part that can be used with both
voltage and current output DACs and is used for conditioning in DACs and ADCs circuits - among many other parts. An opamp’s use in your DAC circuit is only limited by your creativity and the constraints of your application. Several excellent opamp textbooks are available for study on this ubiquitous part. When using a buffer, the designer should ensure the opamp circuit’s error contribution is less than 1/2 LSB of the DAC – ideally as low as you can get within reason and cost. Other aspects such as bandwidth, voltage rails, and RRIO performance in an opamp should also be considered in matching an opamp to a DAC.

**PREVENTING NOISE**

There are several ways that noise propagates through a system: Conductive (traces, connections), near field magnetic (transformer, inductor), electric field (capacitors), far field electromagnetic (radio, antennas). For DAC designs, conductive mode accounts for the majority of noise on a circuit board. The other mechanisms and many other techniques for noise mitigation are contained in the one of the best references for a circuit designer, “Noise Reduction Techniques” by Henry Ott.

**Traces – conductive noise**

A designer must realize that any signal is a current, which starts from a source of energy and must return to that same source. A diagram of a trace is shown on Figure 6 below. As you can see, it is not merely a wire with some resistance. The trace total impedance must be considered as composition of resistance ($R_E$), including self inductance ($L_E$) and capacitance ($C_E$).

**Figure 5 - Buffering DAC outputs**

**Figure 6 - An actual trace**
For signal frequencies of more than a few KHz, the self-inductance \((L_e)\) becomes a key contributor to noise generation. So, even without considering EMI, all circuits benefit by keeping all loop current paths as short as possible. This reduces the overall inductance and therefore reduces noise. With DAC circuits, you will likely have high speed digital signals on the input side. High speed digital currents should have a short, separate return path back to its source to stop conducted ground noise.

**Grounds**

Perhaps the best definition for a ground is a very low impedance path for current to return to the source. It is the signal return path - as shown on Figure 6 (the dotted line). A dedicated plane on a PCB is a good answer to the definition of a ground. With mixed signal parts like DAC, however, a single ground plane can allow noise from digital circuits to couple into analog signal return paths through the ground plane. One technique to prevent this is to split the ground plane into digital and analog areas and then connect them with a thin trace. This maintains equivalent potential across the ground, but also keeps the digital ground currents away from the analog side. A another option is to use two internal layers - one dedicated to analog ground, the other to digital ground with a via joining them. All things considered, this is a better solution, but it does add to board cost.

**Power Supply Bypassing**

Bypass capacitors on a DAC’s input power pins can reduce noise, and are especially important if switching power supplies are being used. A designer should plan to evaluate capacitors of various values to filter out the range of harmonic noise expected on the circuit. There are two ways to bypass power supplies: Rail-to-Ground (traditional) and Rail-to-Rail (bipolar DACs only). For rail-to-ground bypassing, the designer places several capacitors (0.01\( \mu \)F to 0.1\( \mu \)F in value) as close to the DAC power pin as possible. The Rail-to-Rail technique places a capacitor across the two supply rails. This reduces the number of capacitors, but will require a larger package size due to the higher voltage rating needed. In addition to bypassing, a ferrite bead can also be used the power supply trace to further minimize transient power-supply currents.

**PCB DESIGN RECOMMENDATIONS**

Why is it good to remind readers of key PCB layout recommendations with so many good references available? First, any poor PCB layout will degrade signal integrity across the circuit and leads to issues like ringing, oscillation, overshoot/undershoot spikes, and ground bounce. Secondly, a good PCB layout design will improve the DAC circuit performance and reduce overall design time.

- Use a multilayer board with an internal ground plane(s), digital and analog power planes. This allows for very small current loops across the circuit. If required, use split grounds for analog and digital return paths.
- Design the PCB with controlled impedance traces. Any change in a trace such as width, stubs, corners, and splits can cause mismatched impedance and introduce distortion on the signal.
- Consider adding footprints for small resistors (10-20 ohms) on high speed digital signal traces to reduce the rise times. This is a useful technique if issues such as ground bounce are expected.
- Ensure digital signals with fast edges do not pass under analog circuits, and avoid placing those traces over analog split ground planes.
- Keep clock and data lines separated from analog lines and with short distance as possible (such as on component side).
- If analog and digital traces have to share the same space on the PCB (due to circuit density), plan to use ‘guard traces’ to keep noise from coupling.

DAC circuit design can be very challenging. Just as the DAC is a part of a larger circuit, the electrical design engineer himself is part of larger team that requires good collaboration. Good collaboration within a team is always important for success. In that regard, the last article will cover two larger applications in which DACs play a key role.

Footnotes:
(3) http://www.national.com/an/AN/AN-452.pdf